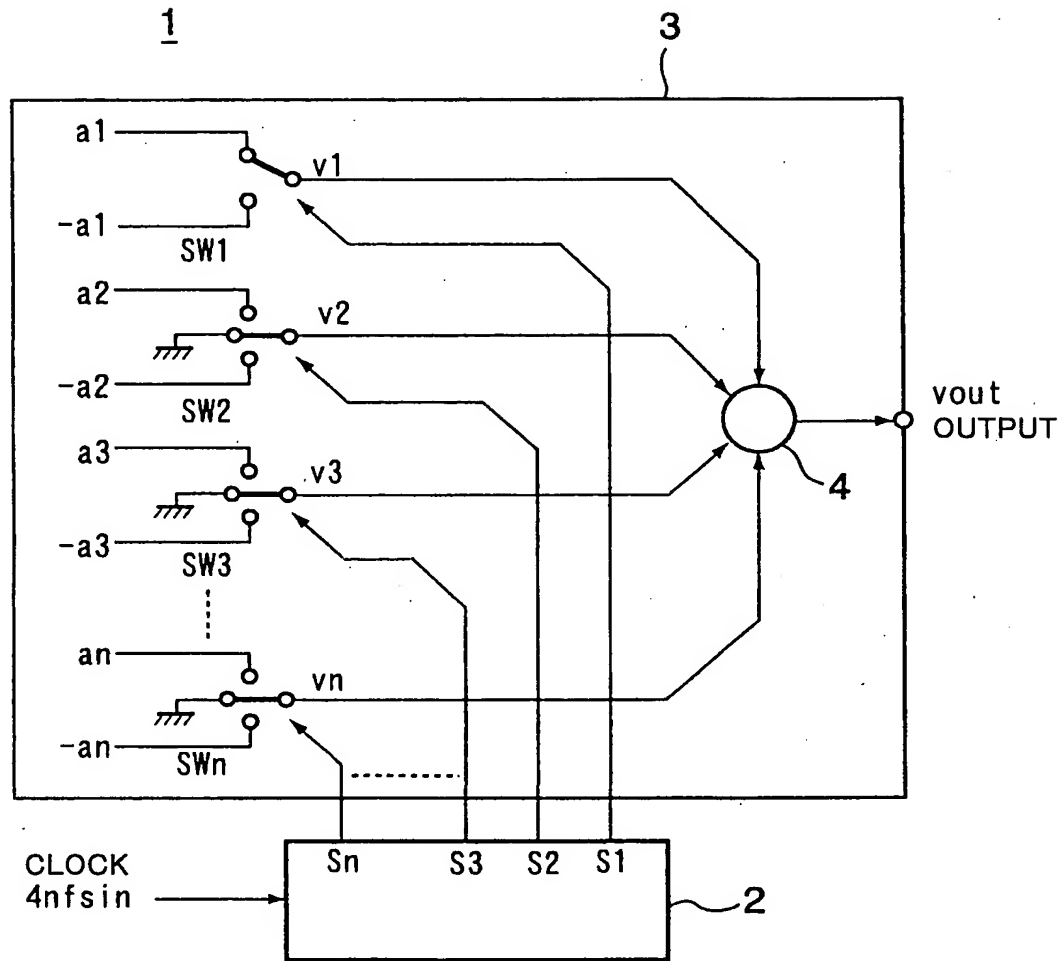
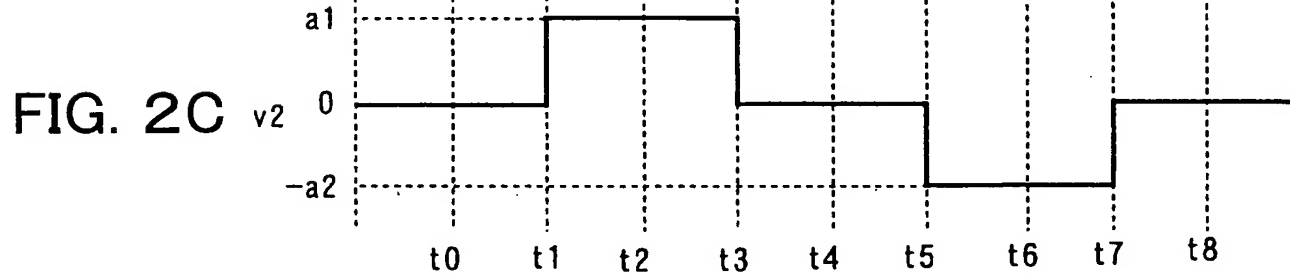
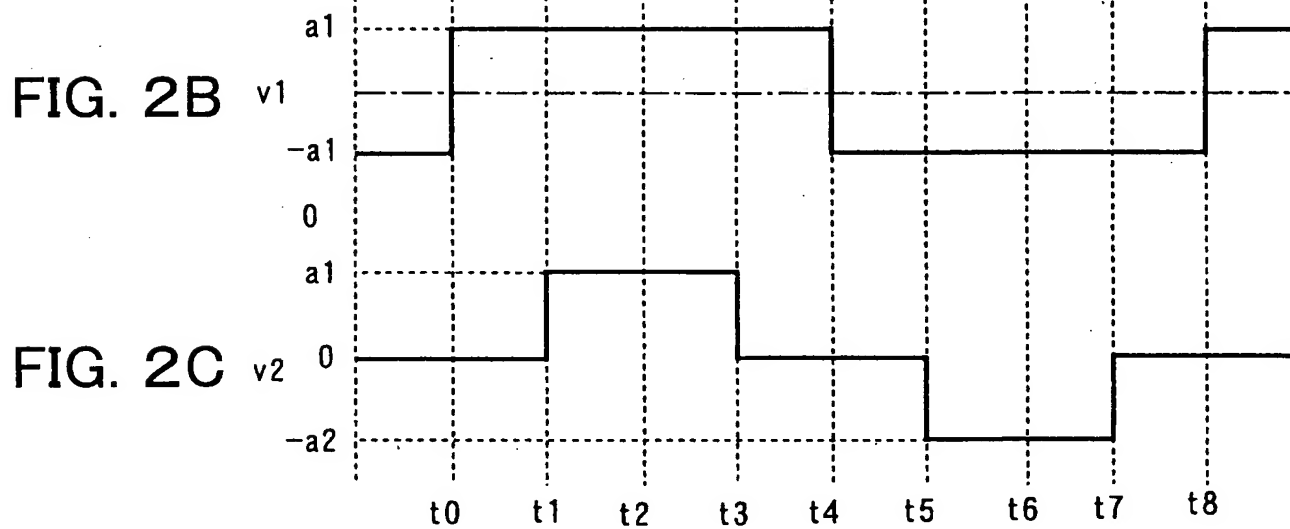
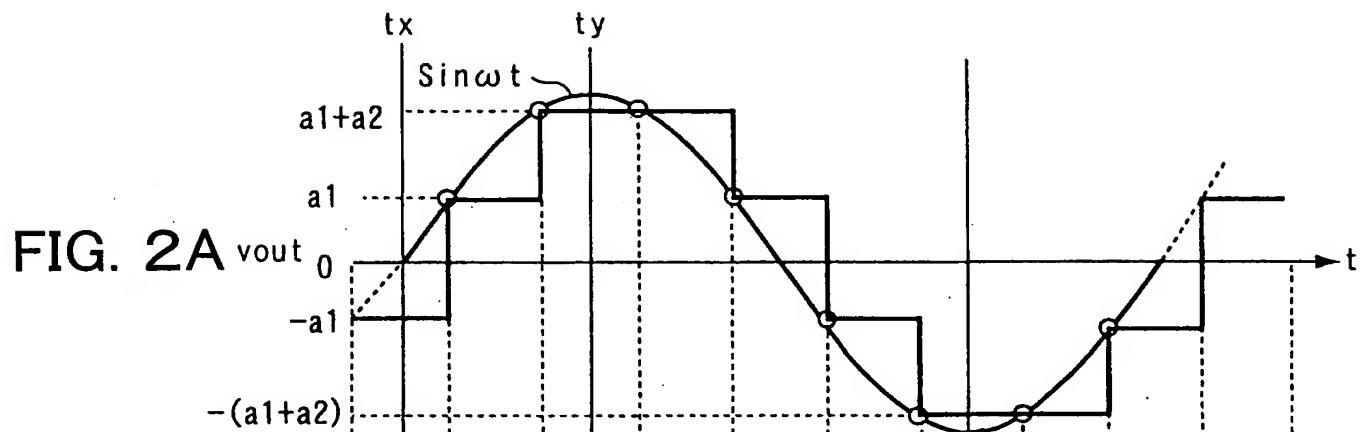
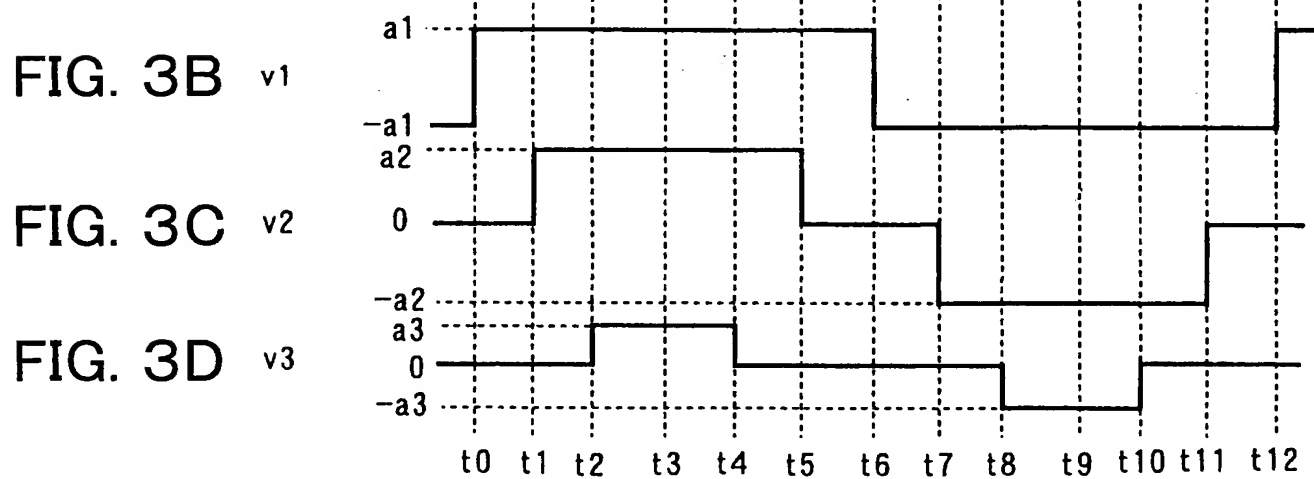
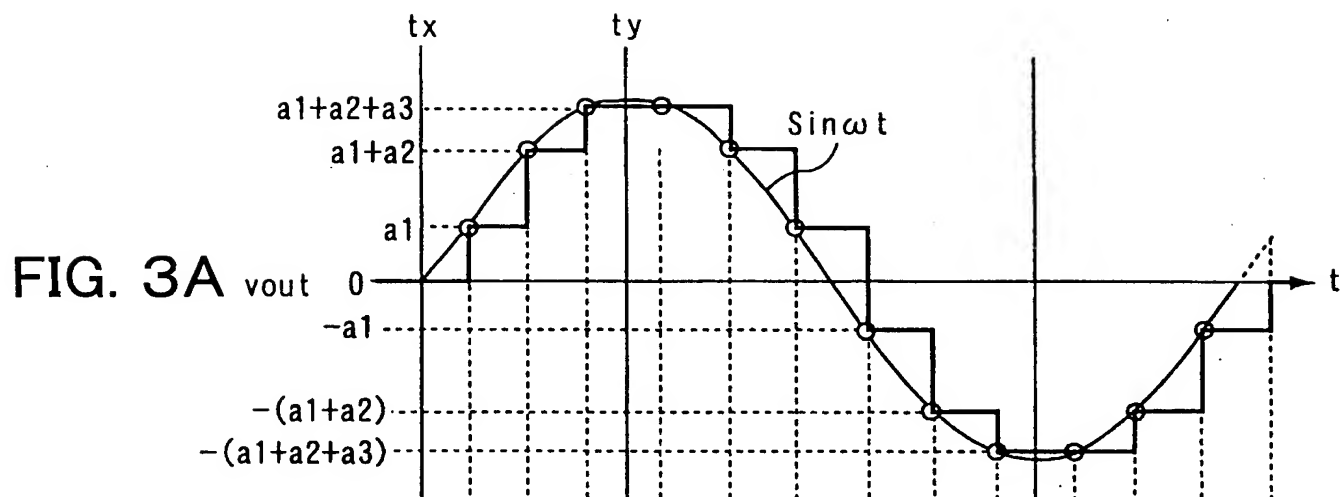


FIG. 1



1 .... SINE WAVE GENERATION CIRCUIT  
 3 .... VOLTAGE OUTPUT CIRCUIT  
 SW1 ~ SWn .... COEFFICIENT GENERATION CIRCUIT





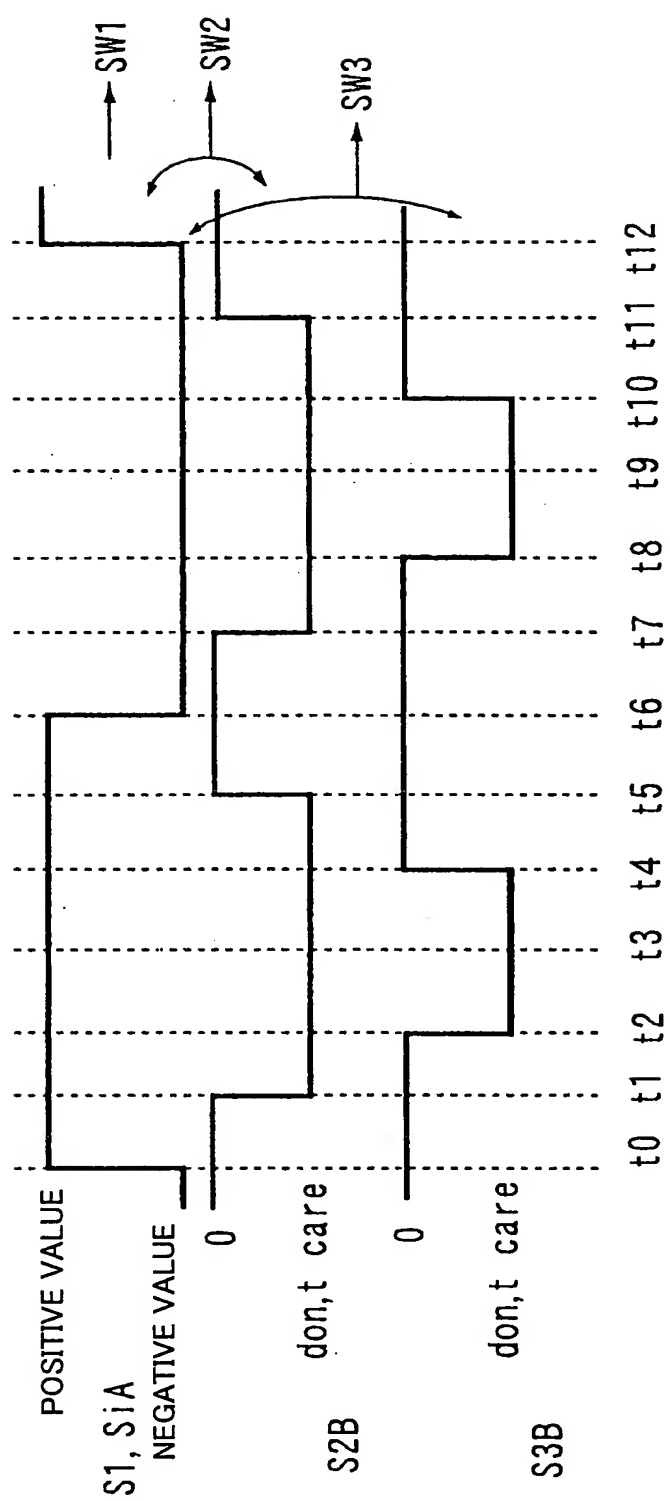


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 5

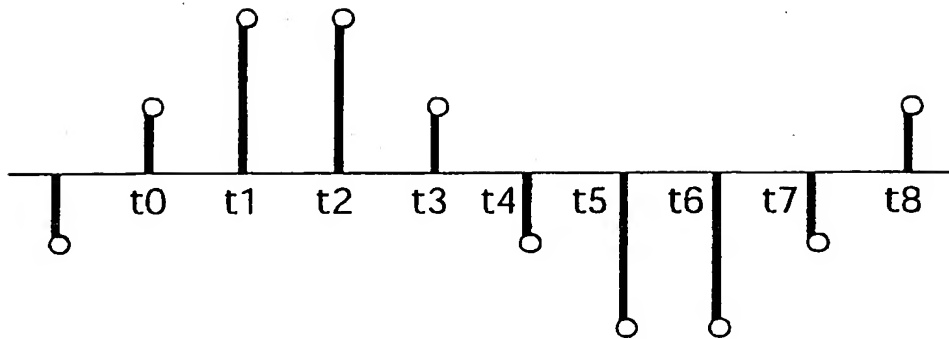


FIG. 6A

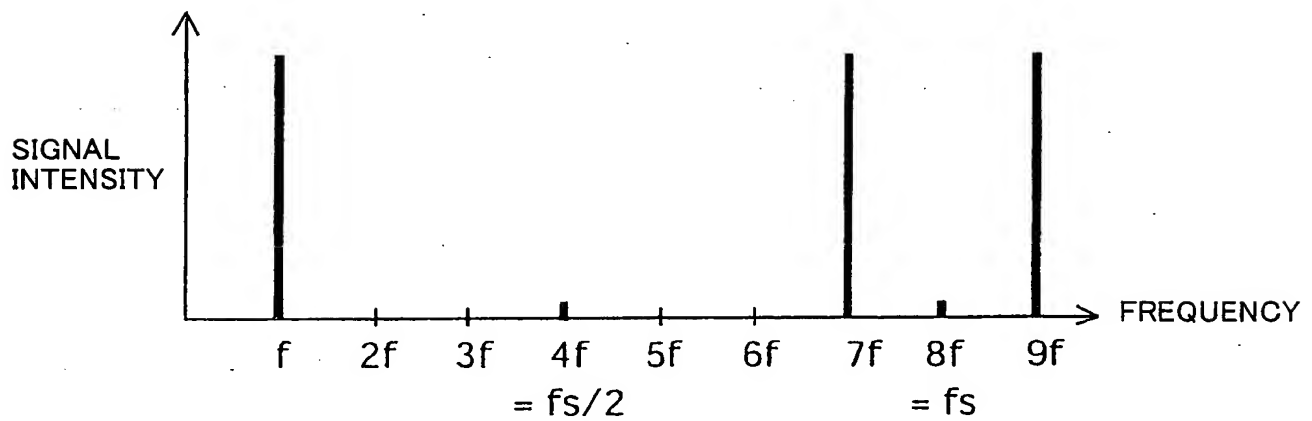


FIG. 6B

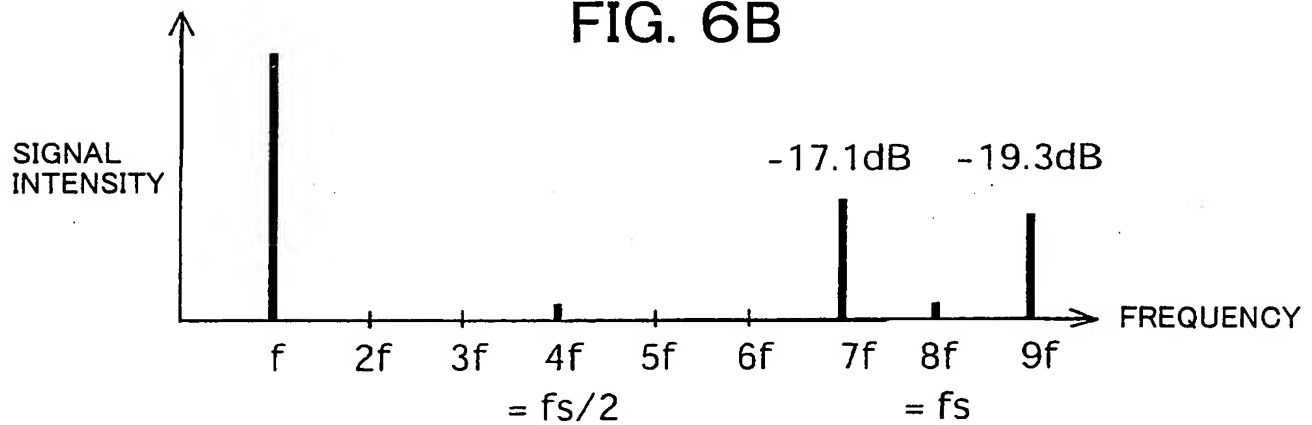


FIG. 7

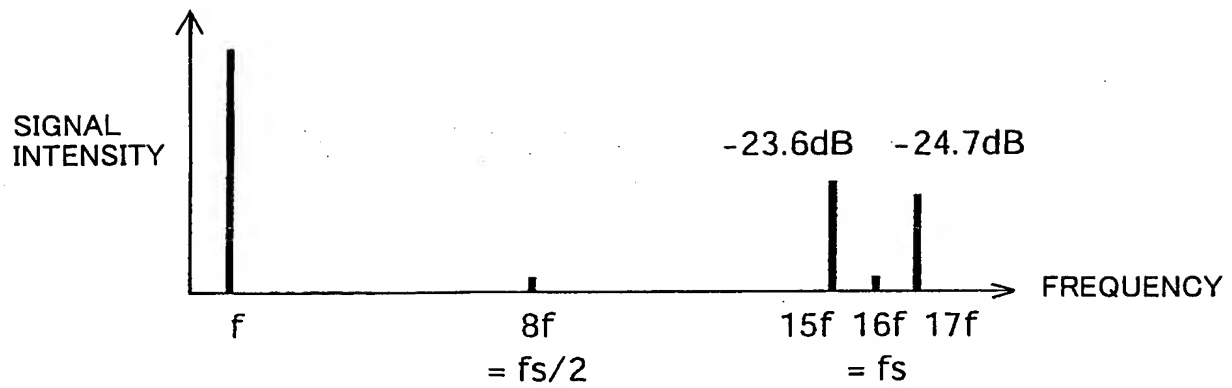


FIG. 8

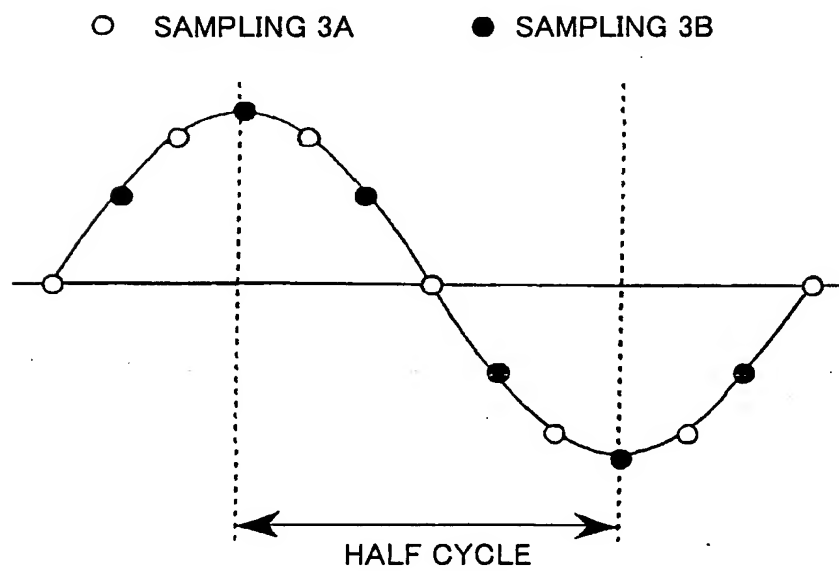


FIG. 9

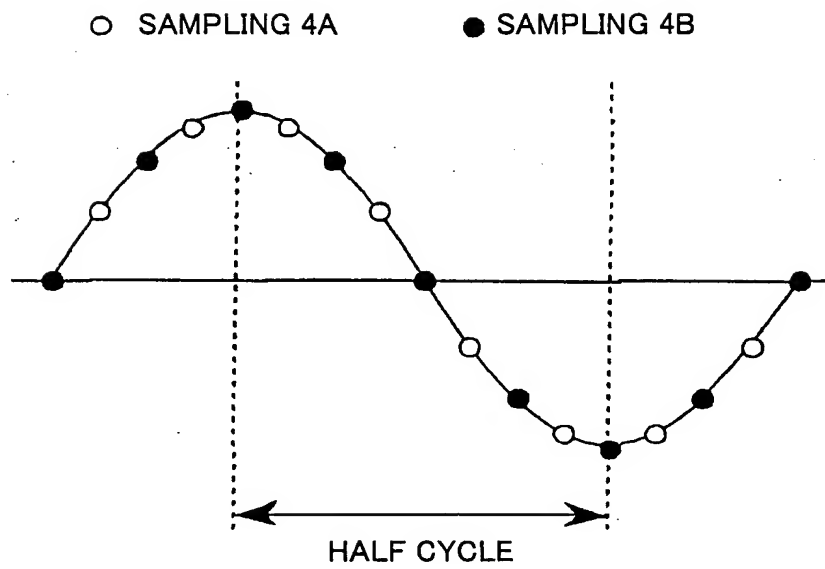
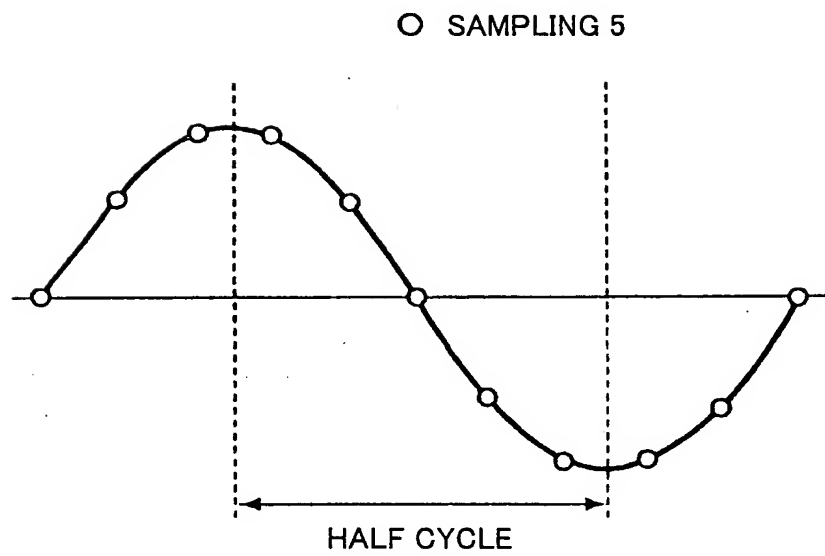


FIG. 10



< SAMPLING 3B >

HALF CYCLE

FIG. 11A  $v_{out}$

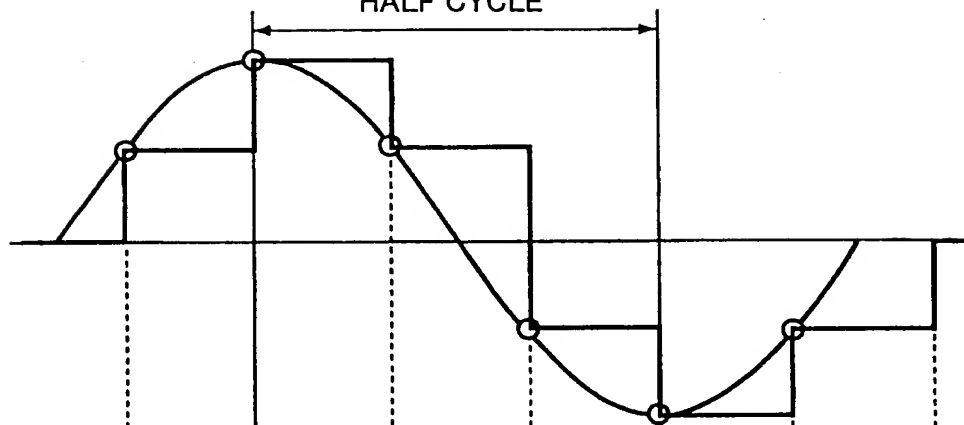


FIG. 11B  $v_1$

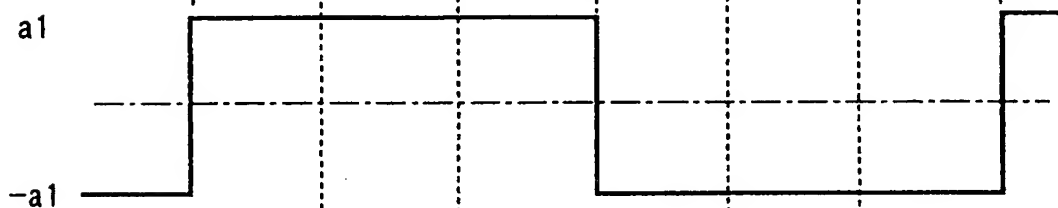


FIG. 11C  $v_2$

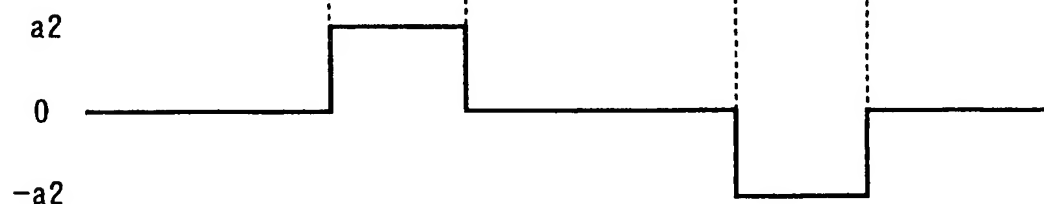




FIG. 12A  $v_{out}$

< SAMPLING 4B >

HALF CYCLE

$a_1$

FIG. 12B  $v_1$

0

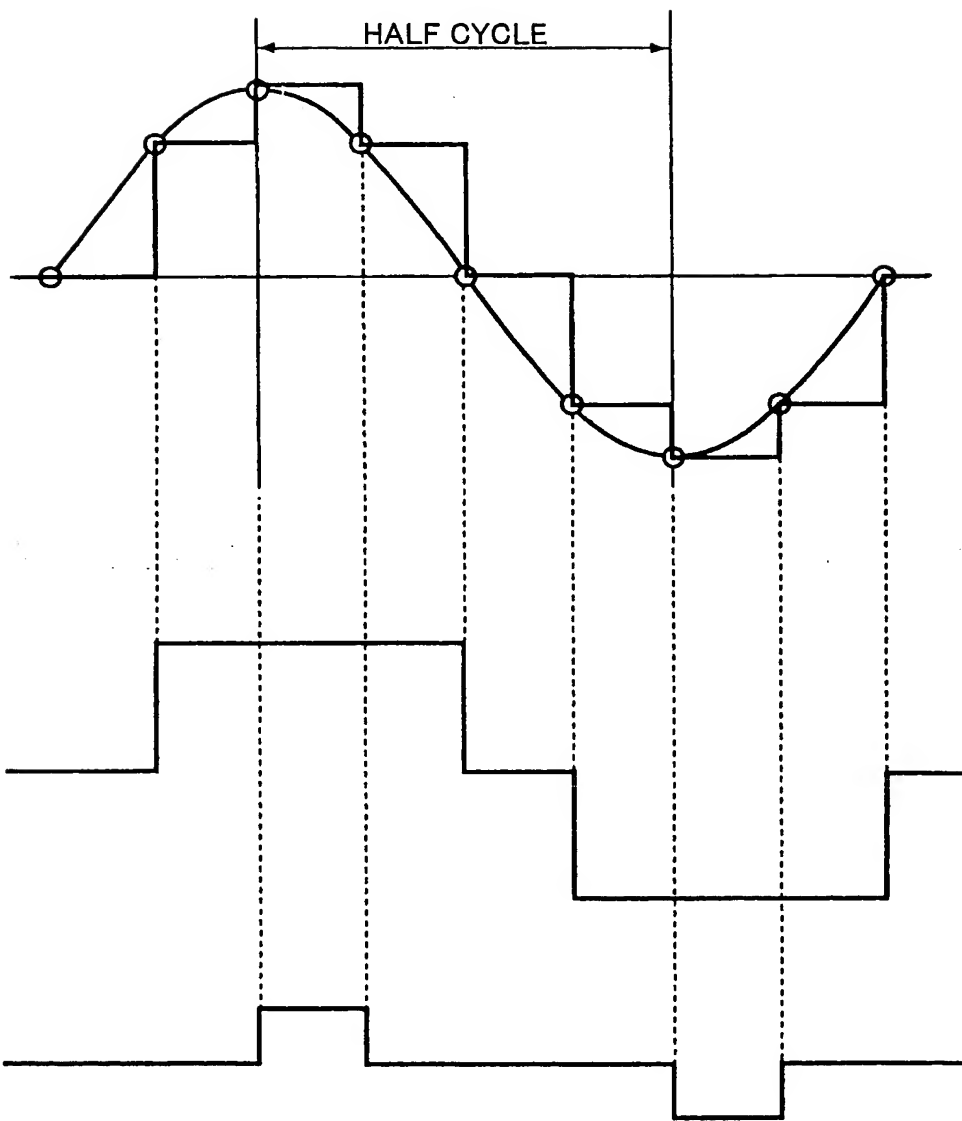
$-a_1$

$a_2$

FIG. 12C  $v_2$

0

$-a_2$



< SAMPLING 5 >

HALF CYCLE

FIG. 13A  $v_{out}$

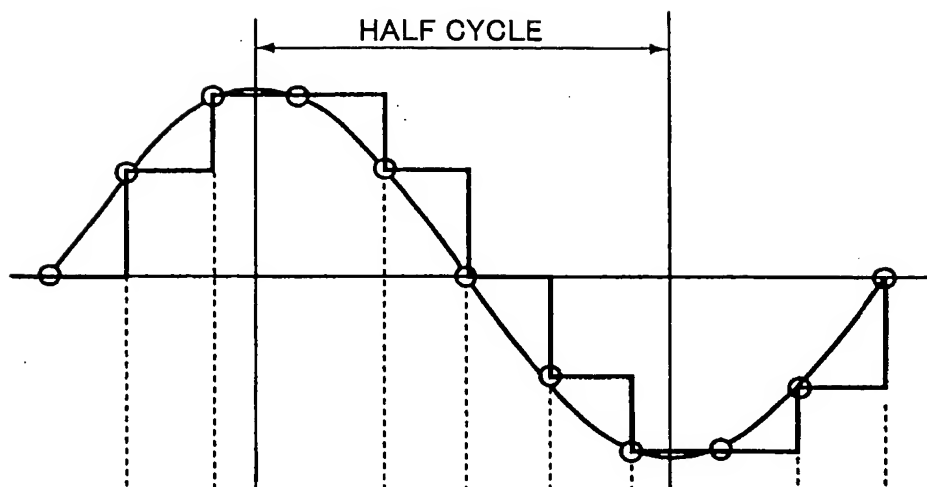


FIG. 13B  $v_1$

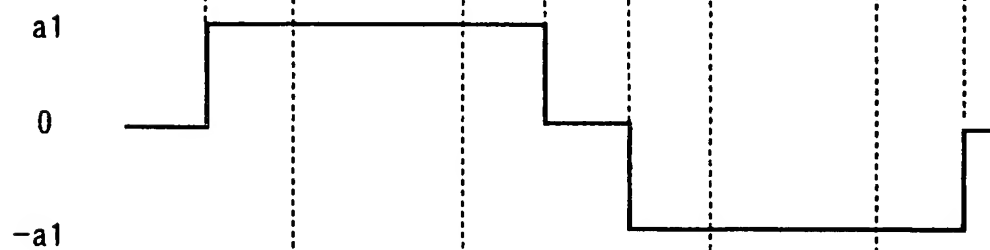


FIG. 13C  $v_2$

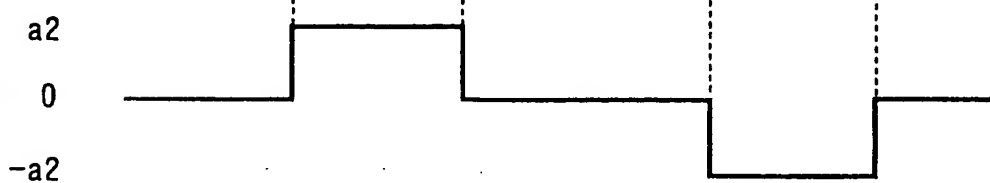


FIG. 14

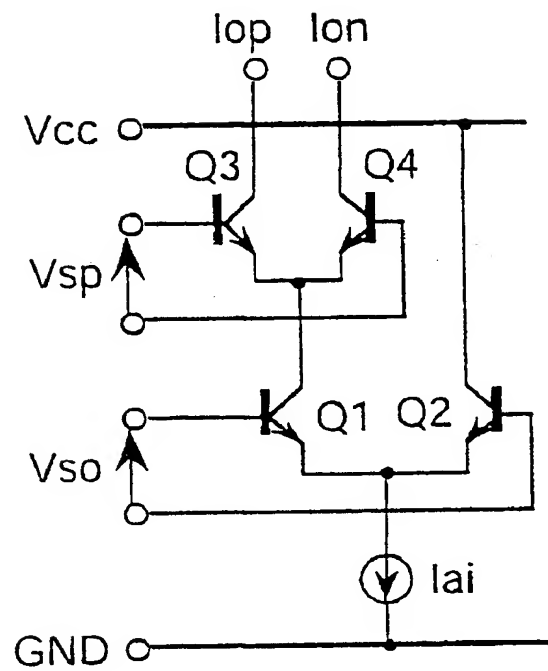


FIG. 15

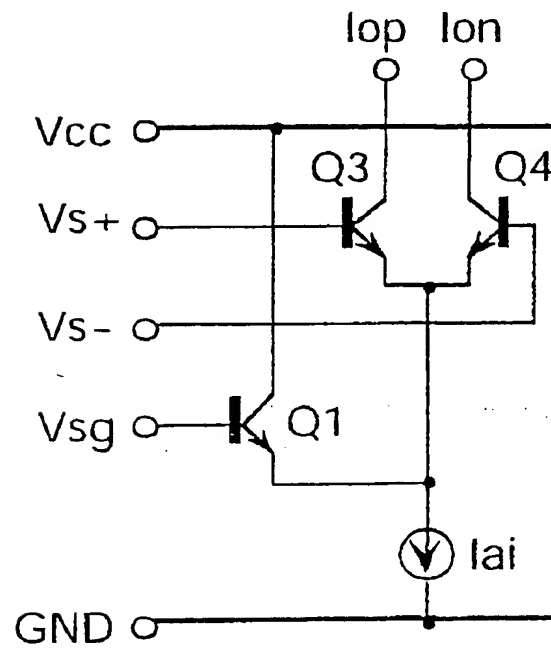


FIG. 16

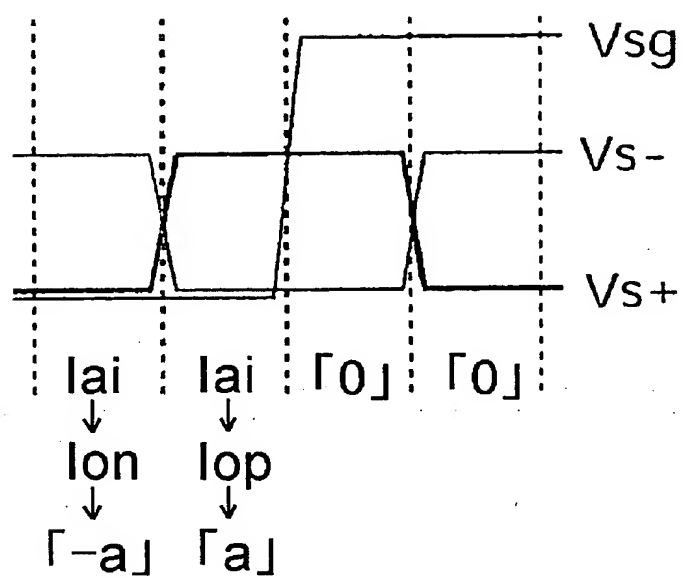
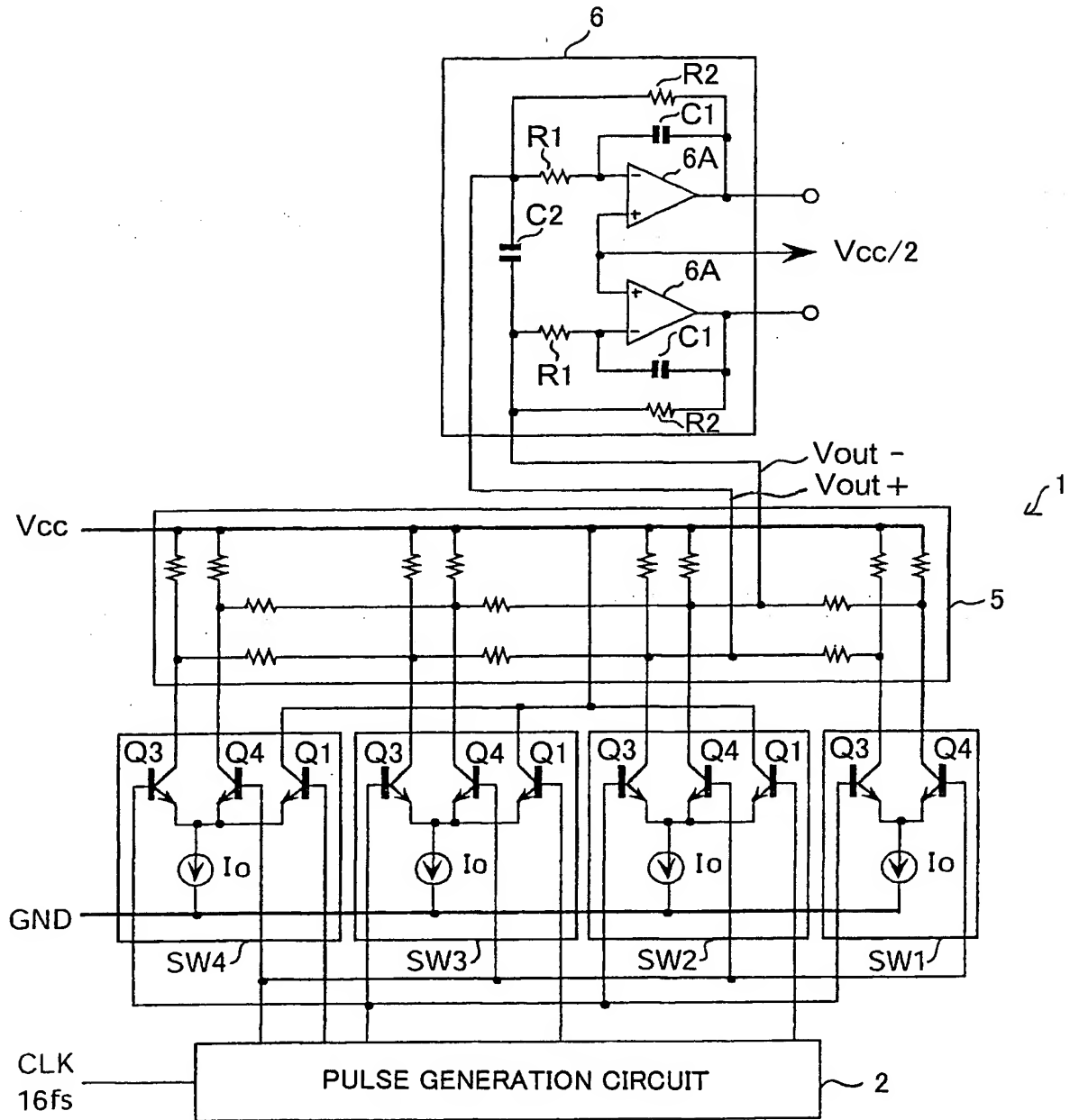


FIG. 17



- 1... SINE WAVE GENERATION CIRCUIT  
 5... RESISTOR LADDER CIRCUIT  
 6... LOW PASS FILTER  
 SW1~SW4... COEFFICIENT GENERATION CIRCUIT

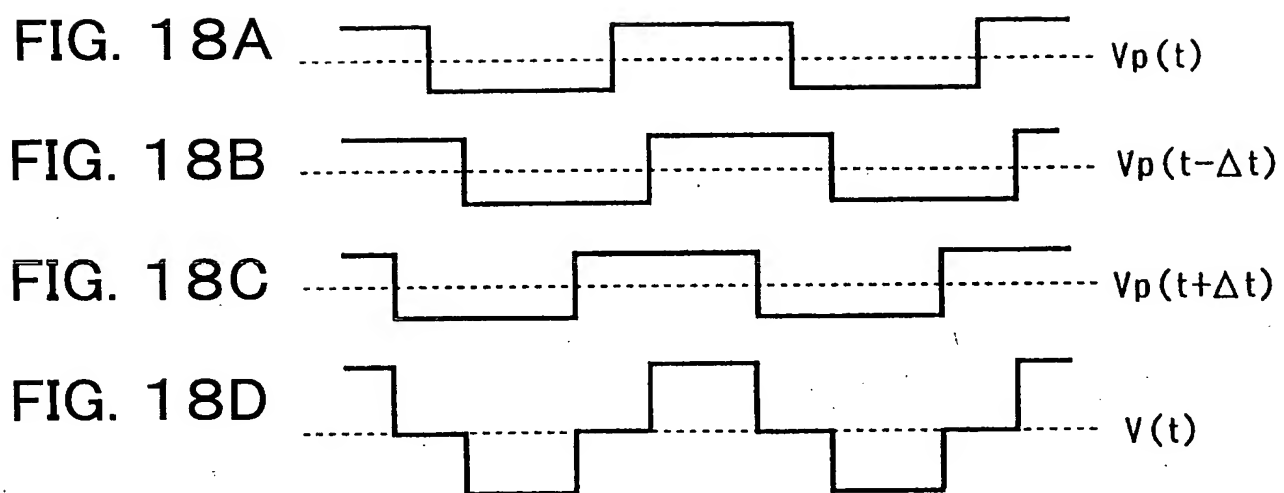
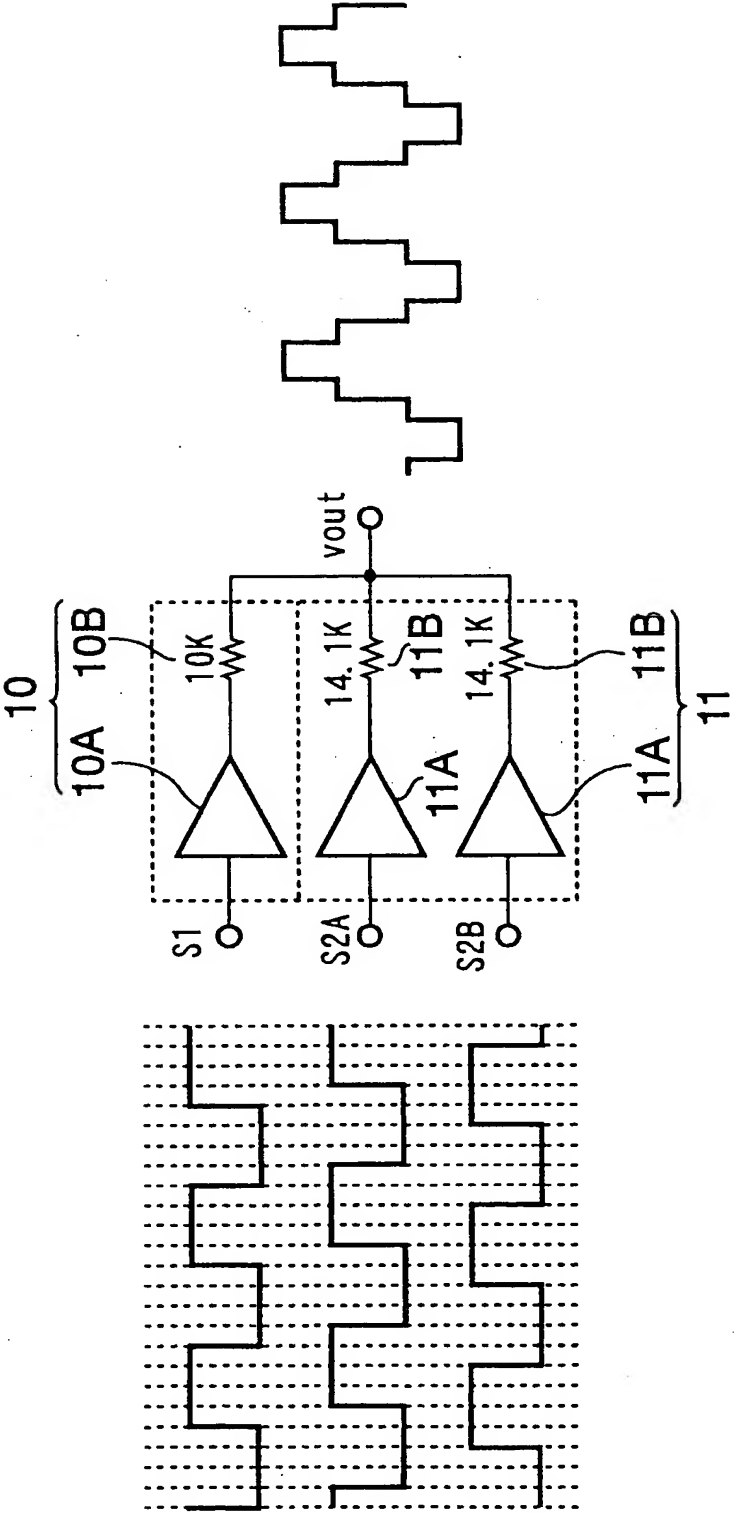


FIG. 19



10 ---- BINARY-VALUE GENERATION CIRCUIT

11 ---- TERNARY-VALUE GENERATION CIRCUIT

FIG. 20

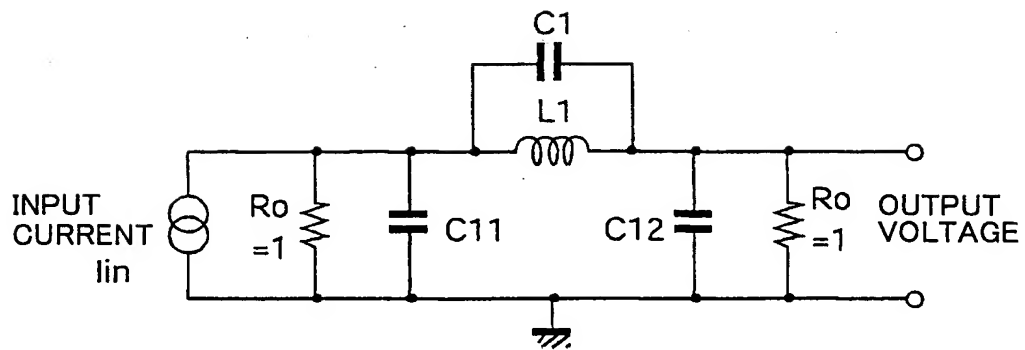


FIG. 21

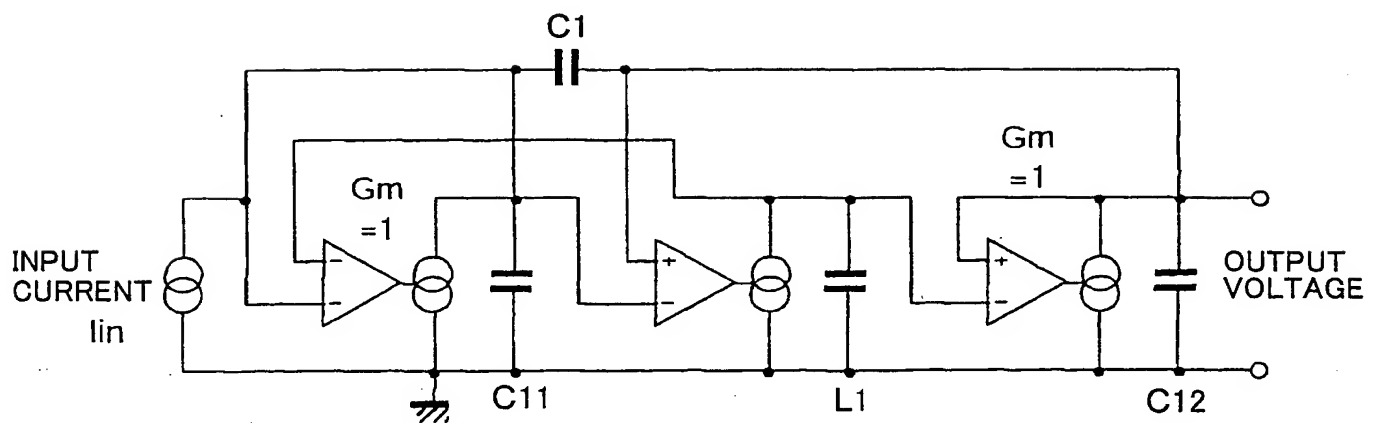




FIG. 22

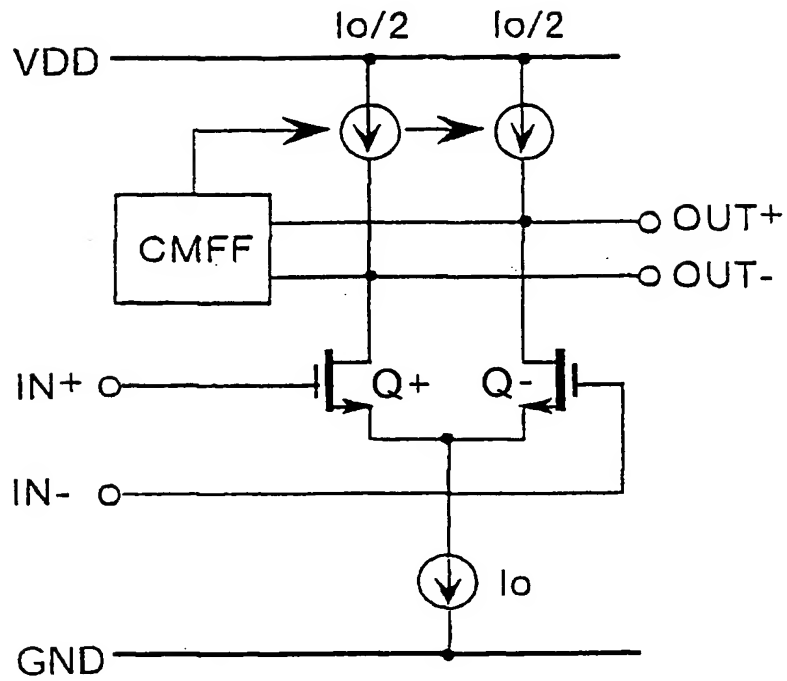


FIG. 23

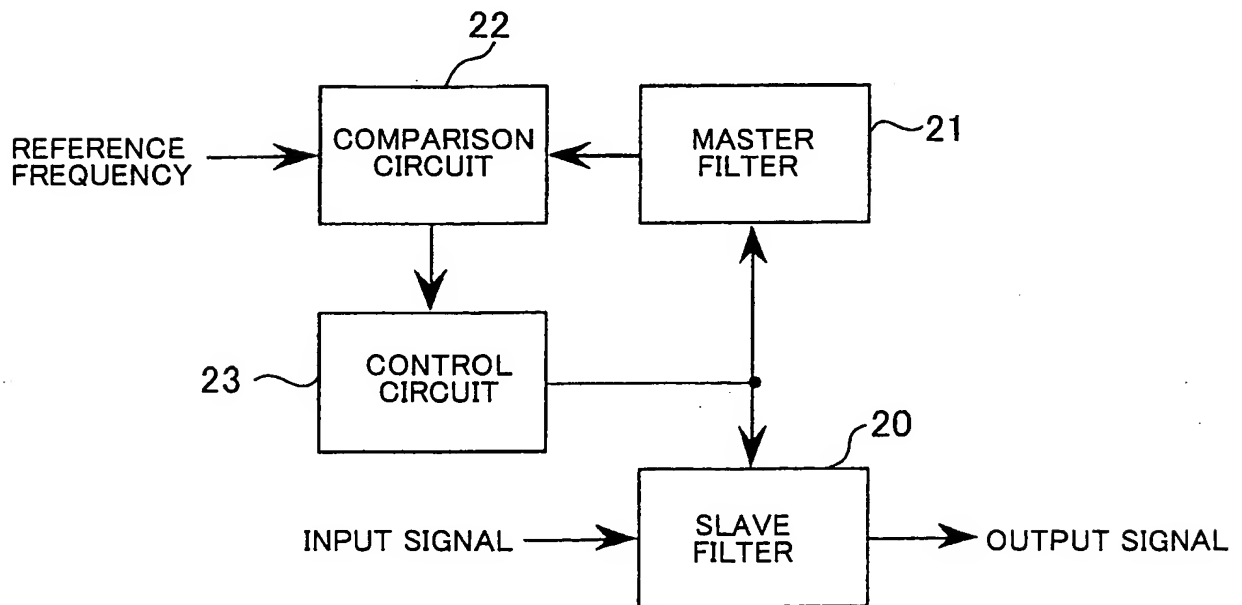


FIG. 24

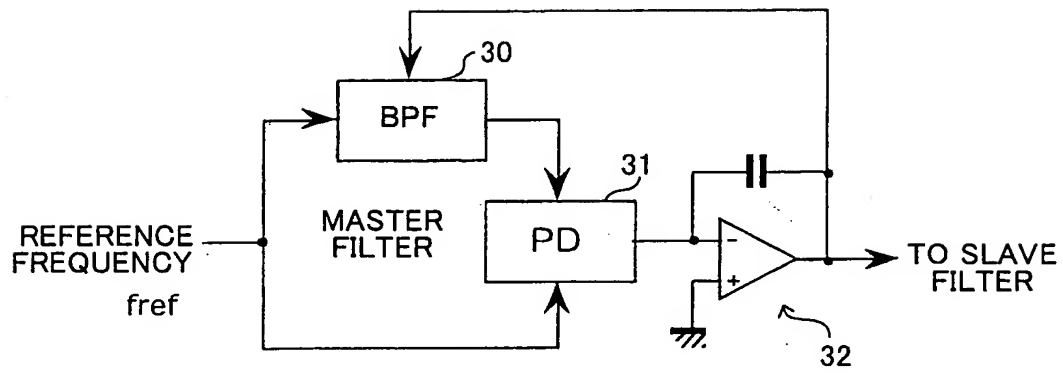


FIG. 25

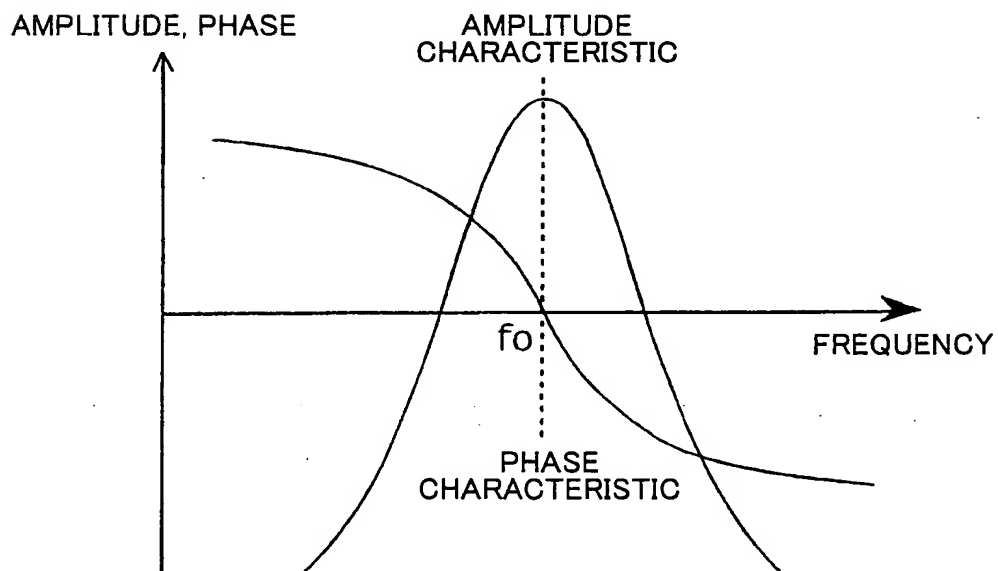
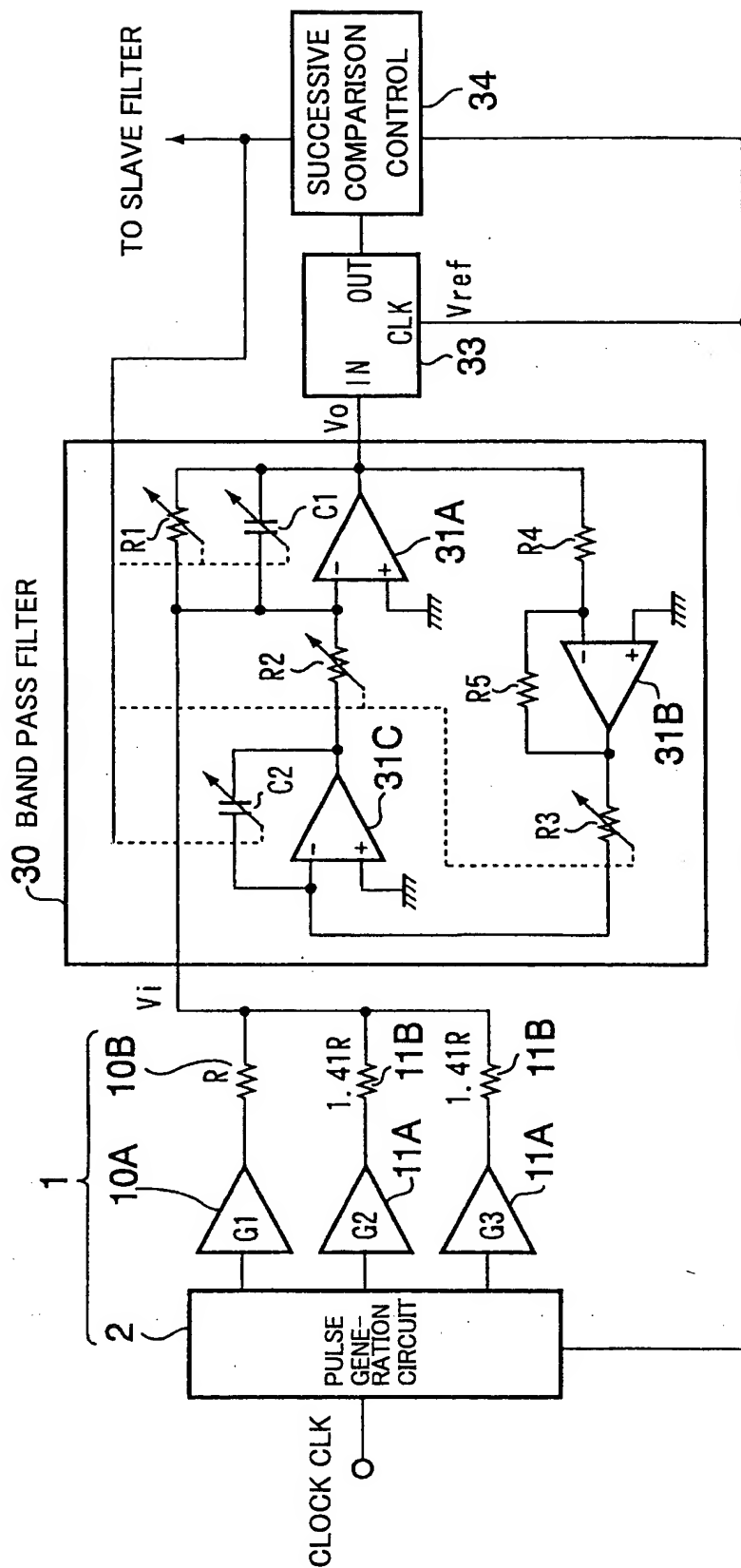


FIG. 26



1 ---- SINE WAVE GENERATION CIRCUIT

10A~10B ---- BINARY-VALUE GENERATION CIRCUIT

11A~11B ---- TERNARY-VALUE GENERATION CIRCUIT

FIG. 27

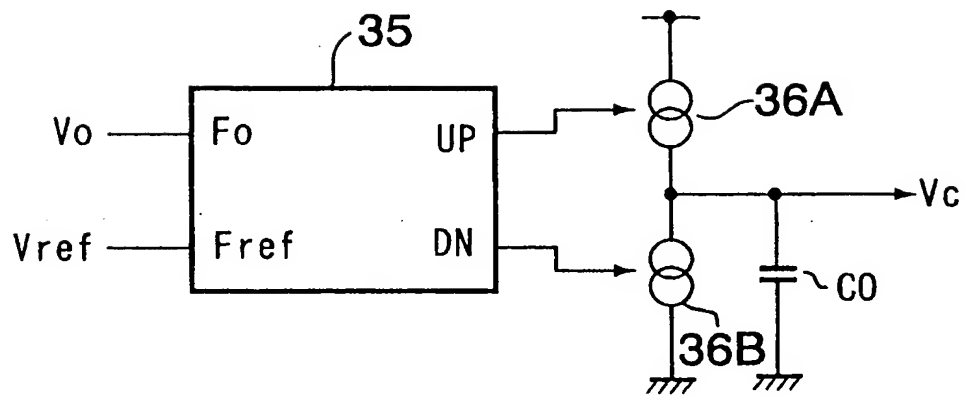


FIG. 28

